Remarks

Claims

Claims 1-16 are pending in the present application. Claims 1-20 stand rejected. Claims 1, 6, 11, and 14 have been amended in this paper.

Claim Rejections – 35 U.S.C. § 102

Claims 1-20 stand rejected under 35 U.S.C. § 102(b) as being anticipated by the I^2C Bus Specification, Version 2.1 (hereinafter "the I^2C Specification"). A telephonic interview was held in this case on December 13, 2004, in which the Examiner and the Attorney for the Applicant participated. In that interview, the Examiner pointed to FIGS. 26 and 27 of the I^2C Specification and stated that they appeared to be similar to FIG. 3B of the present application. Applicant appreciates the opportunity to point out the differences between FIG. 3B and FIG. 26-27 of the I^2C Specification, and the relevance of such differences to the language of the claims as currently presented.

As noted in various places in the I^2C Specification (such as in Section 14), the I^2C protocol recognizes both 7-bit addresses and 10-bit addresses. As indicated in Section 14.2 of the I^2C Specification, FIGS. 26-27 of the I^2C Specification illustrate an example involving 10-bit addresses. As described in the I^2C

specification and shown in FIG. 26 therein, "[w]hen a 10-bit address follows a START condition, each slave compares the first seven bits of the first byte of the slave address (11110XX) with its own address and tests if the eight bit (R/W direction bit) is 0." In other words, at this stage each slave compares only *part* of an I^2C address (namely, the *first seven out of ten bits* of the address it receives) to its own address. Although the I^2C specification states that at this stage "[i]t is possible that more than one device will find a match," this is based on a comparison with *part* of an I^2C address, not a *complete* I^2C address.

The I^2C Specification further states that "[a]ll slaves that found a match will compare the eight bits of the second byte of the slave address (XXXXXXXX) with their own addresses, *but only one slave will find a match*" (emphasis added). The complete 10-bit I^2C address consists of: (1) the final two bits of the first byte of the slave address; and (2) the eight bits of the second byte of the slave address. As clearly stated in the portion of the I^2C specification just quoted, once the slaves have compared the entire 10-bit slave address with their own address, *only one slave will find a match*.

In contrast, claim 1 of the present application as currently presented requires "addressing a first subset of the plurality of devices using a primary address, the primary address including a

complete device address defined according to a protocol associated with the data bus, wherein the primary address is shared by the first subset of the plurality of devices." The I^2C Specification neither teaches nor suggests using a *complete* address, defined according to the I^2C protocol, that is shared by a plurality of devices. Rather, as described above, the I^2C Specification only teaches using a complete I^2C address to address a *single* device. The I^2C Specification fails to teach an express limitation of claim 1, as amended. Claim 1, as amended, therefore patentably distinguishes over the teachings of the I^2C Specification.

Reliance on FIG. 3B of the present application is misplaced, because this figure illustrates an example in which a 7-bit I^2C address is used. This figure therefore differs from FIGS. 26-27 of the I^2C Specification, in which 10-bit addresses are used.

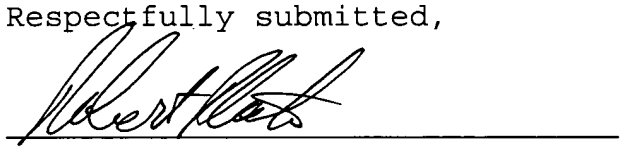
For example, the specification of the present application states on p. 15, lines 21-23, "the first byte of information following the start bit [in FIG. 3A] is a 7-bit address 310 of a possible device on the bus." The same is true of the example illustrated in FIG. 3B of the present application (p. 16, lines 10-15). Element 360 in FIG. 3B is a *complete* 7-bit primary address defined according to the I^2C protocol (p. 16, lines 23-27). Element 360 therefore differs from the seven bits (11110XX) shown in FIGS. 26-27 of the I^2C specification, which represent only *part* of a 10-bit

I^2C address. FIG. 3B of the present application is therefore consistent with and provides support for the above-quoted language in claim 1. Note, however, that claim 1 is not limited to use with 7-bit I^2C addresses.

Claims 1, 6, 11, and 14 have been amended to clarify the above-described distinction between the claimed subject matter and the teachings of the I^2C Specification. Independent claims 6, 11, and 14, as amended, contain the same or substantially the same relevant limitations as claim 1, as amended, and therefore patentably distinguish over the teachings of the I^2C Specification for at least the same reasons. Dependent claims 2-5, 7-10, 12-13, and 15-20 incorporate the limitations of the independent claims from which they depend, and therefore patentably distinguish over the I^2C Specification for at least the same reasons. Applicant therefore traverses the rejection and respectfully requests that it be withdrawn with respect to claims 1-20 as currently presented.

If this response is not considered timely filed and if a request for extension of time is otherwise absent, applicant hereby requests any extension of time. Please charge any fees or make any credits, to Deposit Account No. 08-2025.

Respectfully submitted,



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